

## Experiment (4) Ladder Logic Programming (2)

### Introduction

In the last experiment, basics of ladder logic programming were introduced. In this experiment we are going to study more advanced ladder logic programming instructions; timers, counter and logic operators.

### Objectives

This experiment aims to:

- 1- Introduce the set and reset coil instructions.
- 2- Understand the function of timers, counters and logic operators in ladder logic programming.
- 3- Use timers, counters and logic operators in different applications.
- 4- Be able to perform sequence dependent operations.

### Theory

#### Set Coil Instruction

Figure 1 shows the symbol of set coil instruction:

<address>  
  
---( S )

Figure 1: The symbol of set coil instruction

**Description:** ---( S )--- (Set Coil) is executed only if the RLO of the preceding instructions is "1" (power flows to the coil). If the RLO is "1" the specified <address> of the element is set to "1". An RLO = 0 has no effect and the current state of the element's specified address remains unchanged.

The following example illustrates the operation of set coil instruction, see figure 2:

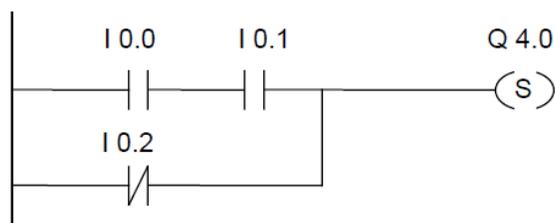


Figure 2: Set coil instruction example

The signal state of output Q4.0 is "1" if one of the following conditions exists:

- The signal state is "1" at inputs I0.0 and I0.1
- Or the signal state is "0" at input I0.2.

If the RLO is "0", the signal state of output Q4.0 remains unchanged.

### Reset Coil Instruction

Figure 3 shows the symbol of reset coil instruction:

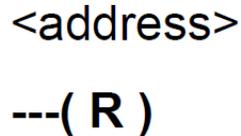


Figure 3: The symbol of reset coil instruction

**Description:** ---( R )--- (Reset Coil) is executed only if the RLO of the preceding instructions is "1" (power flows to the coil). If power flows to the coil (RLO is "1"), the specified <address> of the element is reset to "0". A RLO of "0" (no power flow to the coil) has no effect and the state of the element's specified address remains unchanged.

The <address> may also be a timer (T no.) whose timer value is reset to "0" or a counter (C no.) whose counter value is reset to "0".

The following example illustrates the operation of reset instruction, see figure 4:

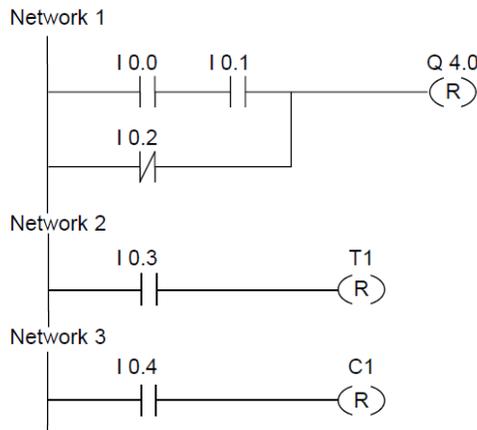


Figure 4: Reset coil instruction example

The signal state of output Q4.0 is reset to "0" if one of the following conditions exists:

- The signal state is "1" at inputs I0.0 and I0.1
- Or the signal state is "0" at input I0.2.

If the RLO is "0", the signal state of output Q4.0 remains unchanged.

The signal state of timer T1 is only reset if:

- the signal state is "1" at input I0.3.

The signal state of counter C1 is only reset if:

- the signal state is "1" at input I0.4..

### On-Delay S5 Timer (S\_ODT)

Figure 5 shows the symbol of on-delay timer.

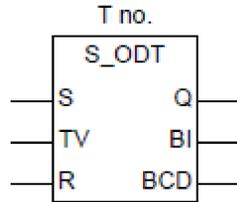


Figure 5: On-delay S5 timer symbol

**Description:** S\_ODT (On-Delay S5 Timer) starts the specified timer if there is a positive edge at the start (S) input. A signal change is always necessary in order to enable a timer. The timer runs for the time interval specified at input TV as long as the signal state at input S is positive. The signal state at output Q is "1" when the timer has elapsed without error and the signal state at the S input is still "1". When the signal state at input S changes from "1" to "0" while the timer is running, the timer is stopped. In this case the signal state of output Q is "0". The timer is reset if the reset (R) input changes from "0" to "1" while the timer is running. The current time and the time base are set to zero. The signal state at output Q is then "0". The timer is also reset if there is a logic "1" at the R input while the timer is not running and the RLO at input S is "1". The current time value can be scanned at the outputs BI and BCD. The time value at BI is binary coded, at BCD is BCD coded. The current time value is the initial TV value minus the time elapsed since the timer was started.

Table 1 illustrates the function of each parameter of on-delay S5 timer:

Table 1: On-delay S5 timer parameters

Parameter	Data type	Description
T no.	Timer	Timer identification number; range depends on CPU
S	Bool	Start input
TV	S5Time	Preset time value
R	Bool	Reset input
BI	Word	Remaining time value, integer format
BCD	Word	Remaining time value, BCD format
Q	Bool	Status of the timer

Figure 6 shows the timing diagram for on-delay S5 timer:

On-Delay timer characteristics:

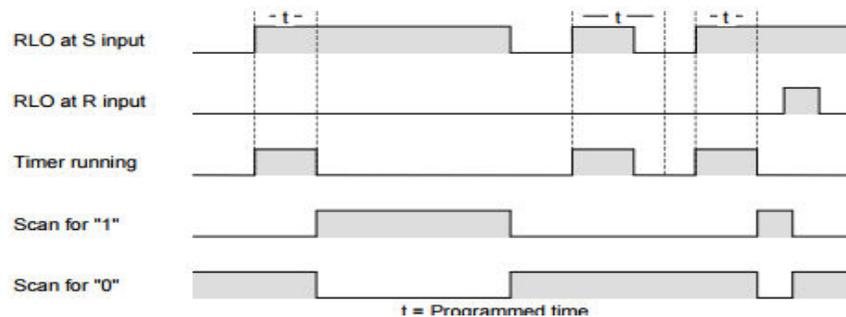


Figure 6: Timing diagram for on-delay timer

The following example illustrates the operation of on-delay timer, see figure 7:

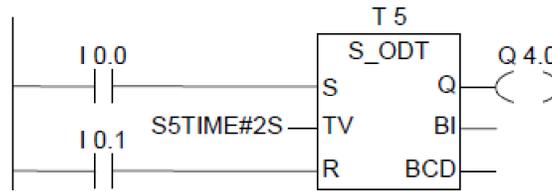


Figure 7: On-delay timer example

If the signal state of I0.0 changes from "0" to "1" (positive edge in RLO), the timer T5 will be started. If the time of two seconds elapses and the signal state at input I0.0 is still "1", the output Q4.0 will be "1". If the signal state of I0.0 changes from "1" to "0", the timer is stopped and Q4.0 will be "0" (if the signal state of I0.1 changes from "0" to "1", the time is reset regardless of whether the timer is running or not).

### Positive RLO Edge Detection

Figure 8 shows the symbol of Positive RLO Edge Detection instruction.

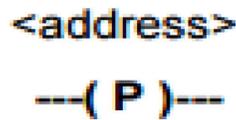


Figure 8: Positive RLO Edge Detection Symbol

**Description:** ---( P )--- (Positive RLO Edge Detection) detects a signal change in the address from "0" to "1" and displays it as RLO = "1" after the instruction. The current signal state in the RLO is compared with the signal state of the address, the edge memory bit. If the signal state of the address is "0" and the RLO was "1" before the instruction, the RLO will be "1" (pulse) after this instruction, and "0" in all other cases. The RLO prior to the instruction is stored in the address.

Table 2 illustrates the function of each parameter of Positive RLO Edge Detection:

Table 2: Positive RLO edge detection parameters

Parameter	Data type	Description
<adress>	Bool	Edge memory bit, storing the previous signal state of RLO

The following example illustrates the operation of Positive RLO Edge Detection, see figure 9:

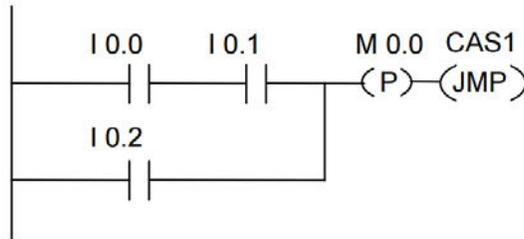


Figure 9: Positive RLO Edge Detection Example

The edge memory bit M0.0 saves the old RLO state. When there is a signal change at the RLO from "0" to "1", the program jumps to label CAS1.

### Negative RLO Edge Detection

Figure 10 shows the symbol of Negative RLO Edge Detection instruction.

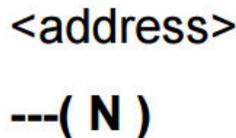


Figure 10: Negative RLO Edge Detection Symbol

**Description:** ---( N )--- (Negative RLO Edge Detection) detects a signal change in the address from "1" to "0" and displays it as RLO = "1" after the instruction. The current signal state in the RLO is compared with the signal state of the address, the edge memory bit. If the signal state of the address is "1" and the RLO was "0" before the instruction, the RLO will be "1" (pulse) after this instruction, and "0" in all other cases. The RLO prior to the instruction is stored in the address.

Table 3 illustrates the function of each parameter of Negative RLO Edge Detection:

Table 3: Negative RLO edge detection parameters

Parameter	Data type	Description
<adress>	Bool	Edge memory bit, storing the previous signal state of RLO

The following example illustrates the operation of Negative RLO Edge Detection, see figure 11:

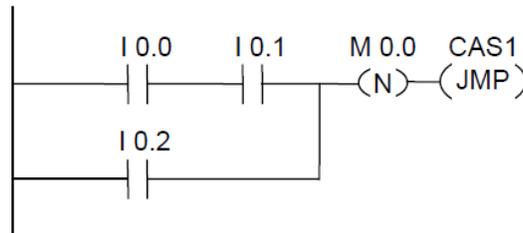


Figure 11: Negative RLO Edge Detection Example

The edge memory bit M0.0 saves the old RLO state. When there is a signal change at the RLO from "1" to "0", the program jumps to label CAS1.